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On July 27, 2001

TOWNSEND and TOWNSEND and CREW LLP

By: Andrea

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PATENT
Attorney Docket No.: A1126/T08910
TTC No.: 16301-008910

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:

KRAMADHATI V. RAVI et al.

Application No.: 09/362,504

Filed: July 27, 1999

For: METHOD FOR REDUCING THE INTRINSIC STRESS OF HIGH DENSITY PLASMA FILMS

Examiner: Rudy Zervigon

Art Unit: 1763

APPELLANT'S REPLY BRIEF UNDER 37 CFR § 1.193(b)(1)

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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Examiner's Answer mailed on May 29, 2001 to the Appeal Brief filed on April 20, 2001, Applicants respectfully request the Board of Patent Appeals and Interferences to consider the following remarks. This appeal brief is filed in triplicate, and is believed to be proper pursuant to 37 CFR § 1.193(b)(1).

ARGUMENTS:

A. The Examiner's Desperate Attempt to Distort the Teaching of Onuki et al. by Relying on an "Imperfect Reality" Argument Is Unavailing

In the Appeal Brief, Applicants establish that the Examiner misconstrues Onuki et al., including the teachings of Fig. 1a,b, to arrive at the erroneous conclusion that Onuki et

al. anticipates claim 16, and bases the rejection of the remaining claims on the misconstruction of Onuki et al.

The Examiner finally realizes the error of his repeated assertion that Onuki et al. teaches maintaining a plasma by coupling sputtering energy into the processing chamber to deposit a first layer of a film on a substrate by sputtering without biasing the plasma toward the substrate and, thereafter, maintaining the plasma by maintaining coupling of the sputtering energy into the chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer.

In the Answer, the Examiner offers the "imperfect reality" argument for the first time. The Examiner argues that "electrical circuits cannot reproduce exact square wave forms due to a required finite time to charge and discharge the circuitry." "As such the rises and drop-offs of the 'square' wave-forms of Figure 1(b) are not completely vertical with infinite slope, these drop-offs must, in reality, have largely positive (rises) or largely negative (drop-offs) slopes less than infinity." Answer, at page 6, lines 10-14.

The Examiner's desperate attempt to distort the teachings of Onuki et al. based on the "imperfect reality" argument has no merit. It is **undisputed** that Onuki et al. specifically discloses terminating the sputtering power during application of the bias voltage. The specific teaching of Onuki et al. does not change simply because the Examiner postulates that there is some overlap, however slight, between the bias voltage and the sputtering power.

More important, the Examiner completely misperceives the issue. The issue is not whether there is overlap between the bias voltage and the sputtering power, but whether Onuki et al. discloses the limitations of claim 16 (as well as several other independent claims). It clearly does not. For instance, claim 16 recites maintaining the plasma by maintaining coupling of the sputtering energy into the substrate processing chamber and biasing the plasma toward the substrate to deposit a second layer of the film over the first layer. Onuki et al. discloses terminating the sputtering power during application of the bias voltage, so that it does not maintain coupling of the sputtering energy during biasing of the plasma to deposit a second layer. Even the finite drop-off of the sputtering power would presumably reach zero during biasing of the plasma in Onuki et al., so that the sputtering power would not be maintained.

On the other hand, if the circuitry were so imperfect that some finite sputtering power would be maintained during application of the biasing voltage, then there would inevitably be some finite bias voltage during application of the sputtering power as well. As such, the "imperfect reality" interpretation of Onuki et al. would mean that Onuki et al. cannot meet the limitation of maintaining the plasma to deposit a first layer by sputtering without biasing the plasma toward the substrate, due to the overlap between the bias voltage and the sputtering power.

In sum, not only does the Examiner's "imperfect reality" argument have no basis for altering the teachings of Onuki et al., but Onuki et al. does not anticipate claim 16 and does not disclose the features of the remaining independent claims under the Examiner's own "imperfect reality" rationale.

B. The Examiner Has Not Demonstrated That the Claimed Product Can Be Made by Another Process

The Examiner asserts that claims 16 and 23 are product-by-process claims, and states that no patentable weight is accorded the process limitations in claims 16 and 23 on the ground that "if the examiner can demonstrate that the product as claimed can be made by another materially different process such as conventional sputtering (Jin Onuki et al – Figure 1a) vs. Switching bias sputtering (Jim Onuki et al – Figure 1b); defining the product in terms of a process by which is it made is nothing more than a permissible technique that applicant may use to define the invention." Answer, at page 7, lines 9-13.

The Examiner alleges that the switch biasing sputtering shown in Fig. 1(b) of Onuki et al. anticipates claim 16. It appears the Examiner is alleging that the product as claimed can be made by the conventional sputtering shown in Fig. 1(a) of Onuki et al. The Examiner has no basis for this allegation. Significantly, even Onuki et al. itself states that the two techniques are different and produce different films:

> The reason why the concentrations of impurities in the films deposited by conventional d.c. bias sputtering are much higher than those for films by conventional d.c. sputtering is thought to be the result of simultaneous progression of sputtering and bias sputtering. Therefore, the authors have developed a one-step switching bias

sputtering method in which d.c. sputtering and d.c. bias sputtering are operated alternately in order to enhance both the step coverage and the quality of Al films [2]. As predicted above, the reliability and quality of Al films were found to be superior to those of Al films by conventional d.c. bias sputtering. However, the electromigration resistance of Al films formed by one-step switch bias sputtering was also found to be insufficient compared with those of conventional d.c. sputtering. This is because Al films were contaminated with Ar for a bias of above 100 V, even when the bias was applied intermittently.

This report is focused on the forming conditions of Al films by switching bias sputtering as a means to obtain high-quality films with both high electromigration resistance and step coverage. Effects of two-step bias application and the number of switching cycles on the quality and electromigration resistance of Al films were also investigated.

In view of the foregoing, Applicants respectfully submit that the Examiner's unsubstantiated allegation that the product as recited in claims 16 and 23 can be made by another materially different process such as conventional sputtering is without merit.

C. The References Do Not Render Claim 23 Obvious

Claim 23 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Ye et al. in view of Onuki et al., Boys et al., Ramarotafika et al., and Matsuura. Applicants respectfully assert that these claims are patentable over the references because, for instance, the references do not teach or suggest an insulating layer formed between the metal layer and the semiconductor substrate and including a first silicon oxide layer and a second silicon oxide layer deposited using a high-density plasma chemical vapor deposition process, where the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer. In the Answer, the Examiner maintains that claim 23 is obvious over the references.

Although Onuki et al. at Fig. 4 shows a SiO_2 layer, it is "thermally grown," not by high-density plasma chemical vapor deposition process. In addition, Onuki et al. does not

teach or suggest two silicon oxide layers, wherein the first silicon oxide layer is deposited for the reduction of mechanical stress in the second silicon oxide layer. The references do not, individually or combined, teach or suggest depositing first and second silicon oxide layers by high-density plasma chemical vapor deposition, where a first silicon oxide layer deposited for reduction of mechanical stress in the second silicon oxide layer.

For at least the foregoing reasons, Applicants respectfully assert that claim 23 is patentable.

CONCLUSION:

In view of the foregoing, Applicants respectfully submit that the claims are in condition for allowance, and respectfully request that the rejection of these claims be reversed.

Respectfully submitted,

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